CLAIMS:

1. - 9. (Cancelled).

10. (Previously Presented) A method for generation of instruction words in a digital processor having an instruction word memory wherein instruction words are arranged in rows, each instruction word having a plurality of instruction word parts, each driving a functional unit of said processor, comprising:

deriving primary instruction words from a program code;

combining said primary instruction words into a sequence of associated program words;

reading an instruction word from a row of said instruction word memory determined by a reading row number;

modifying said read instruction word by substituting an instruction word part with an information part of an associated program word;

writing said modified instruction word part to a row of said instruction word memory determined by a writing row number; and

outputting a completed instruction word to drive said functional units of said processor,

wherein said reading row number and said writing row number are provided by respective reading row and writing row registers, and wherein a number of sequential reading row and writing row numbers are determined by contents of a block length register.

11. (Previously Presented) A method as specified in claim 10, further providing re-setting contents of said reading row register, said writing row register and said block length register by providing a program word having a set bit, which in an active state designates information parts of said program word as containing data for re-setting said registers.

12. (Previously Presented) A method as specified in claim 11 wherein said active state of said set bit causes said information parts of said program word to be stored in said registers.

13. (Currently Amended) A method as specified in claim 10 wherein said instruction register further includes a first instruction word page and a second instruction word page having the same row numbers, wherein there is provided a page ~~registers~~ register whose contents designate one of said pages as active.

14. (Previously Presented) A method according to claim 10 wherein if an instruction word is not called for during execution of a step of said instruction word generation, an additional instruction word is formed by a prefetch unit calling a subsequent sequence of associated program words.

15. (Previously Presented) A method for the generation of instruction words in a digital processor having an instruction word memory wherein instruction words are arranged in rows, each instruction word having a plurality of instruction word parts, each driving a functional unit of said processor, comprising:

deriving primary instruction words from a program code;

assembling said primary instruction words into a sequence of associated program words;

reading an instruction word from a row and page of said instruction word memory determined by a reading row number and a page number stored in a page register;

modifying said instruction word by substituting an instruction word part with an information part of an associated program word;

writing said modified instruction word to a row and page of said instruction word memory determined by a writing row number and a page number stored in said page register; and

outputting a completed instruction word to control said functional units of said processor.

16. (Currently Amended) A method according to claim 15 wherein an interrupt signal during execution of a first task by said ~~processor~~ processor, wherein said instruction words are stored in a first page of said instruction word ~~memory~~ memory, causes said processor to generate instruction words using a second page of said instruction word memory for ~~an interrupt~~ a second interrupt task, and on completion of said second interrupt task to return to said instruction words stored on said first page of said instruction word memory.

17. (Previously Presented) A method according to claim 15 wherein if an instruction word is not called during execution of a step of said instruction word generation, an additional instruction word is formed by a prefetch unit calling a subsequent sequence of associated program words.

18. (Currently Amended) ~~In a digital processor wherein instruction words are stored in an instruction word memory having row addresses, the improvement wherein said instruction word memory is addressed by an address generation unit.~~

An arrangement for the generation of instruction words for driving functional units in a processor, the arrangement comprising:

an instruction word memory assigned to the functional units; and

an instruction word buffer for storing previously used instruction word parts having a width which is at least equal to the bit width of the instruction words,

wherein the instruction word buffer comprises a memory with random or fixed-programmed row-by-row access, and wherein the instruction word memory is addressed by an address generation unit to recall previously used instruction word parts.

19. (Currently amended) ~~The improvement specified in arrangement of claim 18 wherein said address generation unit includes a read pointer register, an associated read pointer up/down counter, a write pointer register and an associated write pointer up/down counter, wherein said counters providing counting in accordance with the contents of a block length register.~~

Arrangement of claim 18, wherein the generation unit comprises a block length register, a read pointer register, and a write pointer register and wherein the read pointer register and the write pointer register are assigned respective up/down counters whose ring counting properties are determined by the content of the block length register.